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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,462	07/03/2003	William B. Andrews	1054.025	6540

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MENDELSOHN AND ASSOCIATES PC
1515 MARKET STREET
SUITE 715
PHILADELPHIA, PA 19102

EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,462	ANDREWS ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8,10 and 15-21* is/are rejected.

7)☒ Claim(s) *4,5,7,9 and 11-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/3/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 8, 10, and 15-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen et al. (US 6,686,769 B1, "Nguyen", hereinafter).

Regarding claim 1, Nguyen discloses a programmable logic device (PLD)(col. 4, lines 64+), comprising a logic core (120; col. 4, lines 64+); connected to an input/output (I/O) interface (100), the I/O interface comprising one or more programmable I/O buffers (PIBs)(200, 300), wherein:

at least one PIB can be programmed to perform two or more of:

(a) a double data rate (DDR) input mode (200) in which an incoming DDR data signal (I/O pin 110) is converted into two single data rate (SDR) data signals (Input A, Input B; see Fig. 5) that are made available to the logic core;

(b) one or more demux input modes (200) in which an incoming data signal (I/O pin 110) is demultiplexed into two or more lower-rate data signals (Input A, Input B; see Fig. 5) that are made available to the logic core;

(c) one or more DDR demux input modes in which an incoming DDR data signal is converted into four or more lower-rate SDR data signals that are made available to the logic core; and

(d) one or more additional input modes (201-203; col. 5, lines 36+) in which an incoming data signal is made available to the logic core without any demultiplexing or DDR-to-SDR conversion (via 240); and

the at least one PIB can be programmed to perform two or more of:

(a) a DDR output mode (300) in which two SDR data signals (Output A, Output B) from the logic core are converted into a single outgoing DDR data signal;

(b) one or more mux output modes in which two or more data signals from the logic core are multiplexed into a single, higher-rate, outgoing data signal (I/O Pin 110);

(c) one or more DDR mux output modes in which four or more SDR data signals from the logic core are converted into a single, higher-rate, outgoing DDR data signal; and

(d) one or more additional output modes in which a data signal (Output A) from the logic core is provided as an outgoing data signal without any multiplexing or SDR-to-DDR conversion (via top input line of 340).

Regarding claim 2, Nguyen discloses that the PLD is a field programmable gate array (FPGA) (col. 4, lines 64+).

Regarding claim 3, Nguyen discloses that the one or more additional input modes comprise a pass-through data input mode (see output of 203) and an input register mode (see output 208); and

the one or more additional output modes comprise a pass-through data output mode (see Output A via 340) and an output register mode (see Output A via 310).

Regarding claim 6, Nguyen discloses that the PIB supports a plurality of different demux input modes (ZBT/SDR input), a plurality of different DDR demux input modes (DDR iput), a

plurality of different mux output modes (ZBT/SDR output), and a plurality of different DDR mux output modes (DDR output) (see col. 8, line 15 through col. 11, line 28).

Regarding claim 8, Nguyen discloses that to support the input modes, the PIB comprises:

(1) a DDR stage adapted to convert an incoming DDR data signal (I/O Pin) into two SDR data signals (Input A, Input B); and

(2) a shift stage (220, 230) and an update stage (280, 290) adapted to demultiplex one or more data signals into two or more lower-rate data signals (see Fig. 5).

Regarding claim 10, Nguyen discloses that the PIB further comprises a transfer stage (240, 250) adapted to apply a time-domain transfer to one or more data signals (Input A, Input B).

Claims 15 and 16 are essentially the same in scope as apparatus claim 1 and are rejected similarly.

Regarding claim 17, Nguyen discloses a programmable logic device (PLD)(col. 4, lines 64+), comprising a logic core (120; col. 4, lines 64+); connected to an input/output (I/O) interface (100), the I/O interface comprising one or more programmable I/O buffers (PIBs)(200, 300), wherein at least one PIB comprises a transfer stage (330) adapted to apply a time-domain transfer (see clk of 335) to one or more data signals (Output A, Output B).

Regarding claim 18, Nguyen discloses that the transfer stage is adapted to be driven by a system clock signal (clk), corresponding to the time domain of the logic core.

Regarding claim 19, Nguyen discloses additional circuitry (360, 310, 320) within the at least one PIB is adapted to be driven by another clock signal (output of 360) different from the system clock signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nguyen et al. (US 6,686,769 B1, "Nguyen", hereinafter).

As applied previously, Nguyen teaches all the features of the claimed invention, with the exception of teaching the claimed demultiplexing circuitry programmable to demultiplex two SDR data signals into two or more lower-rate SDR data signals; or multiplexing circuitry programmable to multiplex four or more outgoing SDR data signals into two higher-rate SDR data signals.

However, it is well known in the art that logic blocks of the FPGA can be programmed to shift signals via demultiplexer into lower-rate signals or to shift signals via multiplexer into higher-rate signals by using well known rate shifting techniques.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to shift the SDR data signals of Nguyen into lower-rate data signals or higher-rate data signals for many different engineering purposes.

Allowable Subject Matter

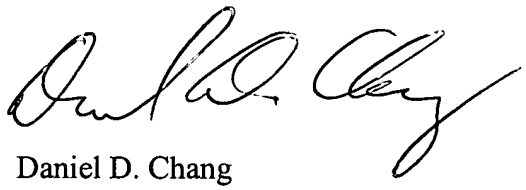
Claims 4, 5, 7, 9, and 11-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER